Attorney Docket No.: 9180-24. PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Glenn A. Rinne Conf. No. 3798
Application No.: 10/689,976 Group Art Unit: 2811
Filed: October 21, 2003 Examiner: Junghwa M. Im
For: STACKED ELECTRONIC STRUCTURES INCLUDING OFFSET SUBSTRATES
Date: June 1, 2007

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NOTICE OF APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Pursuant to 35 USC § 134, 37 CFR § 41.31, and MPEP § 1205, the Applicant in the above-identified patent application hereby appeals to the Board of Patent Appeals and Interferences from the Office Action dated March 6, 2007 at least twice rejecting or finally rejecting claims 1-4, 6-19, 21, 29-31, 33-40, 52, 62, 64-71.

☐ Enclosed is a check in the amount of $_____ for the Appeal fee as provided by 37 C.F.R. § 41.20(b)(1).

☐ Please first reapply any previously paid notice of appeal fee and appeal brief.

☐ Payment by credit card is requested. Form PTO-2038 is attached.

☐ A petition for an extension of time under 37 CFR § 1.136(a) is enclosed.

☒ Also enclosed: Pre-Appeal Brief Request for Review and Reasons in Support of Pre-Appeal Brief Request for Review

☒ The Commissioner is authorized to charge $500.00 for the Notice of Appeal and any additional fees that may be required or credit any overpayment to Deposit Account No. 50-0220.

Respectfully submitted,

Scott C. Hatfield
Registration No. 38,176

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
Customer No. 20792

CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on June 1, 2007.

Signature: Joyce Padi
~~Scott C. Hatfield~~ Joyce Padi

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 9180-24

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on June 1, 2007

Signature: Joyce Paoli

Typed or printed name: Joyce Paoli

Application Number	Filed
10/689,976	10/21/2003

First Named Inventor: Glenn A. Rinne

Art Unit	Examiner
2811	Junghwa M. Im

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [XX] attorney or agent of record. Registration number 38,176
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

Scott C. Hatfield
Typed or printed name

919 854 1400
Telephone number

June 1, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

Attorney Docket No. 9180-24 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Glenn A. Rinne; Conf. No. 3798

Application No.: 10/689,976 Group Art Unit: 2811

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REASONS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

This document supports the Pre-Appeal Brief Request for Review that is filed concurrently herewith along with a Notice of Appeal in compliance with 37 C.F.R. 41.31 and with the rules set out in the OG Notice of July 12, 2005. The Applicant hereby requests a Pre-Appeal Brief Review of the rejections of Claims 1-4, 6-19, 21, 29-31, 33-40, 52, 62, 64-71, and 75-79 which were finally rejected in the Final Office Action mailed March 6, 2007 (the Final Action). The Applicant appreciates the allowance of Claims 22-28, 42-51, 55-60, 63, and 72-74 as indicated in both the Final Action and in the Advisory Action of May 22, 2007 (the Advisory Action).

It is not believed that an extension of time and/or additional fee(s) are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

I. Withdrawal of All Rejections Under 35 U.S.C. Sec. 112, 2nd Paragraph, Is Requested

The Applicant respectfully submits that all claims meet all requirements of 35 U.S.C. Sec. 112 for at least the reasons discussed below.

I(a). Claim 1 Meets All Requirements Of 35 U.S.C. Sec. 112

Regarding Claim 1, the Final Action states that:

> Claim 1 recites the limitation "... the first electrical and mechanical connection bypasses the second integrated circuit substrate... ." However, the instant invention does not disclose the aspect. ... Fig. 5 of the instant invention shows that the signal is coupled to the third integrated circuit substrate through the second integrated circuit substrate.

Final Action, page 2. The Advisory Action further states that:

> ... Fig. 5 and the specification of the instant invention explicitly disclose that the signal pass, that is, the first electrical connection between the first and third IC substrate is

> made through the second IC substrate. Therefore, the first electrical and mechanical connection cannot bypass the second integrated circuit substrate.

Advisory Action, continuation sheet.

In response, the Applicant respectfully submits that support for the recitations of Claim 1 are provided, for example, by the illustrated embodiments of Figure 5 as follows. (*See*, for example, Application, page 14, lines 7-30.) The first integrated circuit substrate of Claim 1, for example, is supported by the substrate 10a of Figure 5; the second integrated circuit substrate of Claim 1, for example, is supported by the substrate 10b of Figure 5; the third integrated circuit substrate of Claim 1, for example, is supported by the substrate 10c of Figure 5; and the first electrical and mechanical connection of Claim 1, for example, is supported by the large bump 50c of Figure 5 (providing electrical and mechanical connection between the substrates 10a and 10c). While the electrical and mechanical connection provided by the large bump 50c is part of a signal path 60 that traverses the substrate 10b in the illustrated embodiment of Figure 5, the electrical and mechanical connection provided by the large bump 50c bypasses the substrate 10b as shown in Figure 5. While other portions of signal path 60 of Figure 5 (which passes through the large bump 50c) may traverse the substrate 10b, the electrical and mechanical connection provided by the large bump 50c bypasses the substrate 10b as shown in Figure 5. Accordingly, the Applicant respectfully submits that Claim 1 meets all requirements of 35 U.S.C. Sec. 112.

I(b). Claim 9 Meets All Requirements Of 35 U.S.C. Sec. 112

Regarding Claim 9, the Final Action states that:

> Claim 9 recites the limitation "... device side ... face a first direction and the backsides face a second direction." Note that the instant invention discloses that both the device side and the backside face the PCB. Claims 15, 21 and 29 recite the similar limitation.

Final Action, page 2. In addition, the Advisory Action states that:

> Note that both of the device side and the backside are a part of the device and the device sides are mounted on the PCB as disclosed in the instant invention. Therefore, both of the front and the back surfaces of the devices face the same direction, that is a top surface of the PCB. (Underline added.)

Advisory Action, continuation sheet. As discussed below, front and back surfaces of an integrated circuit substrate do not face the same direction as asserted by the Advisory Action.

As discussed with respect to Figures 1 and 2a-2b, a device side of a substrate and a backside of the substrate are on opposite sides of the substrate. *See*, Application, page 11, lines 7–14, and page 12, lines 10–17. Accordingly, the device side of the substrate and the backside of the substrate face opposite directions, and the device side of the substrate and the backside of a same substrate cannot both face the printed circuit board as suggested by the Final Action. Moreover, Figure 5 shows that device sides of the substrates 10a, 10b, and 10c face the substrate 210 (such as a printed circuit board PCB), while backsides of the substrates 10a, 10b, and 10c face away from the substrate 210. Accordingly, the Applicant respectfully submits that Claim 9 meets all requirements of 35 U.S.C. Sec. 112. The Applicant further submits that Claims 15, 21, and 29 also meet all requirements of 35 U.S.C. Sec.112. Moreover, the similar recitations of Claim 75 are similarly supported in the application as originally filed.

I(c). Claim 19 Meets All Requirements Of 35 U.S.C. Sec. 112

Regarding claim 19, the Final Action states that the recitation "a direct electrical coupling is provided between the signal path and an electronic circuit of the fifth integrated circuit substrate, and wherein the signal path is free of a direct electrical coupling with any electronic circuit of the third integrated circuit substrate" is not disclosed. *See*, Final Action, page 2. In support of the rejection of claim 19, the Final Action states that:

> ... Fig. 5 of the instant invention shows that the signal is coupled to the third integrated circuit substrate through the fourth integrated circuit substrate.

Final Action, page 2. The Advisory Action further states that:

> It is still confusing to understand this limitation since the referred portion of "Figure 6 at page 16, line 3 to page 18, line 21 of the Application" does not show this aspect at all. Furthermore, the applicant does not provide a clear explanation other than the speculation of "A portion of a signal path 'may' thus be provided on an integrated circuit substrate without providing a direct electrical coupling with any electronic circuit of the integrated circuit substrate." ... In addition, the claim does not recite that "[a] portion of a signal path may thus be provided on an integrated circuit substrate"....

Advisory Action, continuation sheet.

The Applicant respectfully notes that a unique signal path for a memory device is discussed, for example, with respect to Figure 6 at page 16, line 3 to page 18, line 21 of the Application as originally filed. As discussed in the Application as originally filed:

> ... signal paths through traces **30_{8-12}'** may terminate one signal at each level. Accordingly, signal paths including conductive traces **30_{8-12}'** may provide a unique signal path for each substrate for distribution of a unique data input/output and or chip select signal for each substrate. In the example of Figure 6, the bump **50_{12}'** may be coupled to a data input/output or chip select input for the substrate to receive the unique signal for the substrate. In the example of Figure 6, the bumps **40_{7-12}'** and **50_{7-11}'** and the traces **30_{8-12}'** are **electrically isolated from** inputs/outputs of the substrate and merely provide coupling of unique signal paths to other substrates in the stack further from the printed circuit board. (Underline and bold added.)

Application, page 16, lines 19-28. Accordingly, a direct electrical coupling may be provided between a signal path and an integrated circuit substrate in a stack with the signal path being free of a direct electrical coupling with (*i.e.*, electrically isolated from) any electrical circuit of another integrated circuit substrate in the stack. Accordingly, all recitations of Claim 19 are supported in the Application as originally filed. In addition, all recitations of Claims 52 are also supported for reasons similar to those discussed above with respect to Claim 19. While Claim 75 has been grouped with Claim 19 in the Final Action, Claim 75 does not include recitations corresponding to the recitations of Claim 19 to which the Final Action has objected. Accordingly, the Applicant submits that the objections relating to Claim 19 do not apply to Claim 75.

I(d). All Claims Meet All Requirements Of 35 U.S.C. Sec. 112

The Applicant thus submits that all recitations of Claims 1, 9, 15, 19, 21, 29, 52, and 75 are fully supported in the Application as originally filed for at least the reasons discussed above, and withdrawal of all rejections under 35 U.S.C. Section 112 is requested. The Applicant further submits that Claims 9-19, 21, 29-31, 33-40, 52, 62, 66-67, 69-71, and 75-79 are in condition for allowance because all rejections under 35 USC Section 112 have been overcome, and no art rejections have been applied to these claims.

II. Claims 1 And 6 Are Patentable Over The Cited Art

Claims 1 and 6 have been rejected under 35 USC Section 102(e) as being anticipated by U.S. Patent No. 6,392,292 to Morishita (Morishita). The Applicant respectfully submits, however, that Claims 1 and 6 are patentable over Morishita for at least the reasons discussed below. In support of the rejection of Claim 1, the Advisory Action states that Arguments from the Applicant's submission of May 2, 2007, are made without incorporating the rejection based on 35 U.S.C. Sec. 112. More particularly, the Advisory Action states that:

> ... the instant invention does not disclose an electrical connection from the first device to the third device bypasses the second device.

Advisory Action, continuation sheet. As discussed above, however, all recitations of Claim 1 are fully supported in the application as originally filed, and all rejections under 35 U.S.C. Sec. 112 should be withdrawn. Accordingly, Claim 1 recites a first electrical and mechanical connection between first and third integrated circuit substrates with the first electrical and mechanical connection bypassing the second integrated circuit substrate (with the second integrated circuit substrate being between the first and third integrated circuit substrates), and Morishita fails to teach or suggest such a structure.

As shown in Figure 5 of Morishita and as discussed in greater detail in the Applicant's submission of May 2, 2007, all interconnections between the first chip 1 and the third chip 3 of Morishita pass through the second chip 2 of Morishita which is between the first and third chips 1 and 3. Accordingly, Morishita fails to teach or suggest any electrical and mechanical connection between chips 1 and 3 of Figure 5 thereof that bypass chip 2.

Accordingly, the Applicant respectfully submits that Morishita fails to teach or suggest the recitations of Claim 1, and that Claim 1 is thus patentable. Dependent Claims 2-4, 6-8, 64-65, and 68 are patentable at least as per the patentability of Claim 1 from which they depend.

III. Conclusion

The Applicant thus submits that all pending claims in the present application are in condition for allowance, and a Notice of Allowance is respectfully requested in due course.

Respectfully submitted,

Scott C. Hatfield
Registration No. 38,176

Myers Bigel Sibley & Sajovec, P.A.
P. O. Box 37428
Raleigh, North Carolina 27627
Telephone: (919) 854-1400
Facsimile: (919) 854-1401
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Joyce Paoli